circuitry and signals are not particularly important for the invention and conventional means may be utilized. However, in one embodiment of the invention, a specific configuration of input signals are provided for additional functionality, and this configuration of input signals is described within co-pending U.S. Patent Application, Serial No. [[XXX]] 10/604,908 (Attorney Docket Number BUR920030088US1, entitled "Method for Splitting Shift and Scan Paths on Scan Only LSSD Latches" and filed on [[June XX, 2003]] August 26, 2003. The relevant content of that application is hereby incorporated by reference. IDC-A3,AMD,M

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6/7/06 AEG

~~*Please replace paragraph [0029] with the following:*~~

If the MUX selects the fuse latch input, a fuse blow process is indicated for the eFuse circuit as shown at block 431, and fuse blow process is completed before the shifted 1 is passed to the next eFuse circuit. However, when the MUX does not select the fuse [[lath]] latch input, the MUX bypass input is selected and the shifted 1 is sent to the next eFuse circuit as shown at block 429. The processing at the current eFuse circuit then ends, as shown at block 433. IDC-A4,AMD

~~*Please replace the paragraph [0037] with the following:*~~

Figure 3B is a table showing the response of the MUX logic of Figure 3A to the select inputs of the AND logic and the clock time required for passing the shifted 1 through the sequence of eFuse circuits. The MUXes are indicated in each column and the parameter being tabulated [[in]] and shown in their respective rows, each entry now corresponding to the particular MUX. For illustrative purposes, it is assumed that a single clock cycle is required to complete a fuse blow operation at any one of the eFuse circuits at which the blow operation is completed. A bypass of the fuse blow operation is assumed to be almost negligible in terms of time (i.e., 1/100 of the time for the fuse blow). For a fuse with MUXes in bypass preceding it, the fusing time for that fuse will be reduced by the propagation delay of the MUXes. This however is negligible since the MUX delays are less than 1/4 nanosecond each and the fusing time is 200 microseconds. IDC-A5,AMD